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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,873	06/21/2007	Adrian Traskov	AP 10880	4466

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EXAMINER	
MCMAHON, DANIEL F	
ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,873	TRASKOV ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *1-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *09 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/03/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 17 are cancelled.

Claims 18 – 34 are presented for examination.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). A certified copy of application 102004006437.7 GERMANY filling date September 10, 2003 has been placed on the record.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 09, 2006 has been received. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. The claims are objected to because of the following informalities:

Claim 19: “CPU 1” lacks of antecedent basis in the claims.

Claim 22: Ambiguous use of the term “especially”.

Claim 28: “the cache” lacks of antecedent basis in the claims. Claim 28 is dependent on claim 27, 26, and 18.

Claim 32: “RAM 3” lacks of antecedent basis in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language “from/into" is vague.

5. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language “a logic 22, 23" is vague.

6. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language “and/or" is vague.

Prior Art Rejections

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18 – 21, 23, 24, and 29 - 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Hohl et al., U.S. Patent 6,026,501 (herein Hohl).

7. Regarding claim 18, Hohl discloses: an analyzing device for an embedded system (column 24, lines 24 – 33)), comprising: at least one CPU (figure 1, element 2); at least one CPU bus (figure 1, element 25); and at least one memory (figure 1, element 6), including at least one communication module for input or output of analysis data using a test interface (figure 1, element 10), wherein the test interface, in addition to control lines, includes at least one group of data lines transmitting data words and address words alternately or in other succession (figure 1, element DDATA), and information indicating whether data words or address words are transmitted is

transmitted by way of at least one control line (figure 1, element PST) so that content and access operations during an operation time to a describable internal memory as well as I/O access operations of the embedded system can be monitored or logged practically without using basic cycles of the CPU (column 3, lines 54 - 57).

8. Regarding claim 19, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: two or more freely selectable analysis modes (column 12, lines 8 – 15), with the analysis modes differing from each other in the way and extent of participation of the CPU in reading or writing data for analysis purposes (column 12, lines 8 – 15), and wherein depending on the selected analysis mode either all write access operations of the CPU to especially definable address ranges are logged without using basic cycles (column 12, lines 36 – 43), or all read access operations of the CPU are logged (column 11, lines 12 – 16), or direct reading and writing of the CPU from/into an external memory (6) is executed by using basic cycles (column 9, lines 1 – 6).

9. Regarding claim 20, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: the communication module comprises a logic, which independently has access to data or address information through a data connection in order to follow write or read access (figure 1, element 10)

10. Regarding claim 21, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: the communication module is connected to a cache (figure

2, element 70), and data transmitted in write or read access operations can be stored in the cache, and data out of the cache can be output in a buffered manner through the test interface or data can be written into the cache using the test interface, respectively (column 5, lines 22 – 25).

11. Regarding claim 23, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: the data transmission from the communication module to the external memory takes place through a parallel interface (column 15, lines 28 – 31).

12. Regarding claim 24, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: the external memory is connected to a data conditioning device which provides an interface connection for external debugging applications (column 11, lines 12 – 16).

13. Regarding claim 29, Hohl discloses: a method for the analysis of an embedded system with a test interface (figure 1, element 10), the method comprising: in that for the transmission of data through the test interface, a data transmission protocol is used in which data is transmitted in several groups of addresses and data (figure 1, element DDATA).

14. Regarding claim 30, Hohl discloses the limitations of the parent claim, claim 29. Hohl additionally discloses: at least one mode is provided in which analysis data in real

time can be read out of the system (column 11, lines 12 – 16) which comprises at least CPU, data memory, program memory, and I/O element (figure 1), or can be written into the system (column 9, lines 1 – 6), so that the system need not be stopped or interrupted for the analysis (column 3, lines 54 – 57).

15. Regarding claim 31, Hohl discloses the limitations of the parent claim, claim 30. Hohl additionally discloses: the memory content or a correspondingly assessable information of the embedded system is copied in real time completely or partly into an external memory (column 9, lines 1 – 6), with the data being buffered in particular before the action, or the memory content of an external memory or any correspondingly assessable information about the memory content of memory is copied in real time completely or partly into a memory of the embedded system, with the data being buffered in particular before the action (column 10, lines 46 – 53).

16. Regarding claim 32, Hohl discloses the limitations of the parent claim, claim 29. Hohl additionally discloses: only data necessary for debugging is transmitted to the external memory in the event of access operations of the CPU to RAM (column 11, lines 12 – 16).

17. Regarding claim 33, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: write access operations or read access operations of the CPU are logged by means of a cache (figure 2, element 70).

18. Regarding claim 34, Hohl discloses the limitations of the parent claim, claim 18. Hohl additionally discloses: information about the write access operations are written into the cache without additional CPU commands or directly into a communication module, (column 11, 15 – 35) and information about the read access operations is written into the cache with active assistance of the CPU (column 11, 15 – 35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hohl et al., U.S. Patent 6,026,501 (herein Hohl), in view of Shakkarwar, U.S. Patent 5,822,768 (herein Shakkarwar).

20. Regarding claim 22, Hohl teaches the limitations of the parent claim, claim 18. Hohl additionally teaches: the test interface is connected to a test memory arranged outside the embedded system, and the external test memory is especially a central core memory (figure 1; column 10, lines 46 – 53). Hohl does not teach: a dual-port memory.

Shakkarwar teaches: a dual-port memory (abstract).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hohl, an analyzing device for an embedded system, as cited above, with the teaching of Shakkarwar, a dual-port memory. A dual-port memory is a well known design choice in that art, and the combination would yield predicable results.

21. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over, in view of Li, U.S. Publication 2002/0083370 (herein Li).

22. Regarding claim 25, Hohl teaches the limitations of the parent claim, claim 18. Hohl does not teach: the device is in an embedded system which comprises a fully operable microcomputer with at least central processing unit and data memory.

Li teaches: the device is in an embedded system which comprises a fully operable microcomputer with at least central processing unit and data memory. (abstract; figure 1)

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hohl, an analyzing device for an embedded system, as cited above, with the teaching of Li: an embedded system. The combination of a device to analyze an embedded system and an embedded system is obvious to try, and would yield a predictable result. The need to analyze embedded systems for performance is well know in the art. An analysis device is one of a limited number of potential solutions to analyzing performance of an embedded system. One of ordinary

skill in the art, at the time of the invention, would realize the combination would yield predictable results

23. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohl, in view of Grochowski et al., U.S. Patent 6,615,366 (herein Grochowski).

24. Regarding claim 26, Hohl teach the limitations of the parent claim, claim 18. Hohl does not teach: the device is in an integrated microprocessor system for motor vehicles with at least two processor cores, wherein the device is associated with at least one of the processor cores contained therein.

Grochowski teaches: : the device is in an integrated microprocessor system for motor vehicles (abstract) with at least two processor cores(figure 1), wherein the device is associated with at least one of the processor cores (abstract) contained therein (abstract).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hohl, a device for analyzing an embedded system, as cited above, with the teaching of Grochowski, dual processor cores containing the analysis device, for the purpose of increasing reliability of an embedded system (abstract). A dual processor core system for increasing reliability of a system is well known technique in the art. A device to analyze an embedded system is well known in the art. The combination of the well known device and the well known technique would yield predictable results.

25. Regarding claim 27, Hohl and Grochowski teach the limitations of the parent claim, claim 26. Hohl additionally teaches: the first processor core with the complete analyzing device (abstract), an incomplete analyzing device is associated with another processor core in the integrated microprocessor system, having a reduced scope of functions compared to the complete analyzing device (column 4, lines 66 – 67; column 5, lines 1 – 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teaching of Grochowski, as cited above, with the teaching of Hohl, a configurable analyzing device associated with a processor core. Configurability is a known technique to limit functionality of a device, and the combination would yield predictable results.

26. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hohl and Grochowski, in further view of Brenza U.S. Patent 4,797,814 (herein Brenza).

27. Regarding claim 28, Hohl and Grochowski teach the limitations of the parent claim, claim 27. Hohl does not teach: the reduction of the scope of functions involves that the cache provided in the analyzing device has a small number of memory locations and/or a small word width, and/or the test interface is not led to the outside, and/or the test interface does not exist.

Brenza teaches: the reduction of the scope of functions involves that the cache provided in the analyzing device has a small number of memory locations and/or a small word width, and/or the test interface is not led to the outside, and/or the test interface does not exist (column 1, lines 16 – 22).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teaching of Hohl and Grochowski, as cited above, with the teaching of Brenza, caches of varying size and data widths, for the purpose of allowing faster access to memory (column 1, lines 10 – 22). Varying the size and data width of a cache is a well known technique, and the combination would yield predictable results.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John P Trimmings/
Primary Examiner,
Art Unit 2117

Dfm
09/02/08